REMARKS

Claims 1-36 are pending in the present application. Unelected claims 12-25 have been canceled herein without prejudice pending the filing of a divisional application. Claims 1 and 26 have been amended herein. Therefore, claims 1-11 and 26-36 are now pending in the present application. As amended, independent Claims 1 and 26 and also the remaining dependent claims 2-11 and 27-36 are believed to be allowable. Reconsideration is requested.

Claims 1-11 were rejected under 35 U.S.C. 102 (e) as anticipated by Yu, U.S. Pat. No. 6,420,218. This rejection is hereby respectfully traversed.

In the Examiner's remarks, Yu was characterized as providing each of the elements of claims 1-11. In response, Applicants submit that Yu does not show, teach or suggest the elements of Claim 1 and its dependent claims.

Yu acknowledges that in providing current silicon-on-insulator devices, a problem occurs if the semiconductor layer is too thin. This is particularly troublesome for regions such as source or drain regions where silicidation is desirable as silicidation requires a minimal thickness. (Yu, Col. 3, lines 5-13). Yu provides a solution to this problem by forming trenches within the top semiconductor layer of a silicon-insulator-substrate, filling the trenches with insulator, depositing amorphous silicon over the entire substrate including the insulator trenches and then using a laser excimer process for performing a high temperature anneal to cause the deposited silicon to melt. Then the newly deposited silicon is recrystallized to form the silicon layer which eventually will be used in the subsequent process steps. During the final anneal the temperature of the semiconductor layer reaches 1100 degrees Celsius. (Yu, Col. 7, lines 5-25). The method and structure of Yu is similar to the prior art approach discussed in the background section of the instant application, and, as described in the instant application, involves the use of complicated processing steps and very high processing temperatures which are undesirable. (Applicants' specification, paragraph 7.)

In contrast, Applicants' claimed apparatus provides a thicker semiconductor layer in the source and drain regions, which is advantageous for certain processes including silicidation,

without the need for the complex processing and high temperatures of Yu. This is accomplished by using a novel structure which is distinct from that of Yu and the prior art.

As amended herein, Claim 1 specifically recites:

A semiconductor device, comprising:

a layer of dielectric material overlying a substrate;

a dielectric pedestal disposed within and integral to said layer of dielectric material located above remaining portions of said layer of dielectric material and having first sidewalls;

a semiconductor channel region located above said dielectric pedestal and having second sidewalls; and

source and drain semiconductor regions disposed adjacent said first sidewalls of said dielectric pedestal and partially overlying said remaining portions of the layer of dielectric material opposing said channel region and each substantially spanning one of said second sidewalls.

Applicants respectfully submit that the structure disclosed and taught by Yu does not show, teach or suggest the above recited elements of Claim 1, including "... a dielectric pedestal disposed within and integral to said layer of dielectric material located above remaining portions of said layer of dielectric material..." and "... source and drain semiconductor regions disposed adjacent said first sidewalls of said dielectric pedestal and partially overlying said remaining portions of the layer of dielectric material..."

Yu's oxide island material is not "integral to" the dielectric layer as required by Claim 1, nor is it "located above remaining portions of said dielectric layer" as required. Accordingly, reconsideration and allowance is respectfully requested for Claim 1.

Claims 2-11 depend from and recite additional patentable features on the apparatus of Claim 1, while incorporating the novel features of Claim 1. These claims are therefore also each believed to be allowable over the rejection. Reconsideration and allowance are respectfully requested.

Claims 26-36 were rejected by the Examiner under 35 U.S.C. §103 as being made obvious by Yu, et al. in view of Vu, et al., U.S. Pat. No. 5,807,771. This rejection is also hereby respectfully traversed.

In the Examiner's remarks, the Examiner asserted that Yu, et al. provides the features of Claim 26 which are common to Claim 1 (as worded prior to the amendments herein), but acknowledged that Yu does not provide the vias and interlevel dielectric layers recited by Applicants' Claim 26. Vu is then recited solely for teaching the use of vias and interlevel dielectric layers. The Examiner concluded it would be obvious to one skilled in the art to add the vias and interlevel dielectric layers of Vu to the structure of Yu.

Without addressing whether the required motivation to combine these two prior art references together as the Examiner proposes is present, Applicants submit that the relied-upon combination, even if made, cannot obviate the elements of Claims 26-36.

Claim 26 has been amended in a manner similar to Claim 1 to further clarify the recited novel structure of Applicants' invention, and now particularly recites:

An integrated circuit device, comprising:

a semiconductor device, including:

a layer of dielectric material formed over a substrate;

a dielectric pedestal within and integral to said layer of dielectric material and located above remaining portions of said layer of dielectric material and having first sidewalls;

a channel region located above said dielectric pedestal and having second sidewalls; and

source and drain semiconductor regions disposed adjacent the first sidewalls of said dielectric pedestal and disposed partially overlying said remaining portions of said dielectric layer and opposing said channel region and each substantially spanning one of said second sidewalls;

an interlevel dielectric layer located over said semiconductor device; and

vias spanning said interlevel dielectric layer and contacting said source and drain regions.

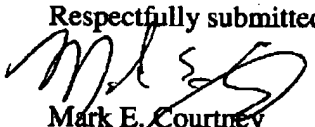
As described above with respect to Claim 1, Yu does not show, teach or suggest the recited elements of "...a dielectric pedestal within said dielectric layer and integral to said dielectric layer and located above portions of said dielectric layer and...." and "...source and drain semiconductor regions disposed adjacent the first sidewalls of said dielectric pedestal and disposed partially overlying said remaining portions of said dielectric layer..."

The added reference, Vu, also does not show, teach or suggest these elements and does not cure the omissions of Yu. Accordingly the proposed combination relied upon in the rejection does not make obvious the structure of Claim 26 and the claim is allowable under 35 U.S.C. §103. Reconsideration and allowance is therefore requested.

Claims 27-36 depend from and recite additional patentable features on the structure of Claim 26 while incorporating the allowable features of Claim 26. For the reasons given herein with respect to Claim 26, these dependent claims are also believed to be allowable. Accordingly, reconsideration and allowance is respectfully requested.

The remarks and amendments herein are believed to place this application in a condition for allowance. Allowance of the claims and timely issuance of the instant application as a patent is therefore respectfully requested. Applicants request that the Examiner contact the attorney by telephone if there are any matters which may be addressed which would expedite the processing of this application.

Respectfully submitted,



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